

**IN THE CLAIMS:**

Please cancel claims 1, 5, and 6 without prejudice to or disclaimer of the subject matter recited therein.

Please amend claim 7 as follows:

**LISTING OF CURRENT CLAIMS**

Claims 1-6. (Canceled)

7. (Currently Amended) An integrated circuit (IC) layout design method utilized for connection of elements in a standard cell, wherein said IC comprises a substrate, said substrate further including pluralities of circuit elements; and m metal layers disposed on said substrate, which are utilized as a connection layout for circuit elements, wherein each metal layer further including an isolation layer for electrical isolation among said metal layers; said IC layout design method comprising the following steps:

arranging a pluralities of circuit ~~passageway~~ passageways at one terminal of a circuit element, said pluralities of circuit passageways extending from said substrate through at least two of said metal layers;

connecting pluralities of lines which are required to be electrically connected to said terminal, to said terminal by connecting said lines to said circuit passageways;

forming an upper metal layer overlying the pluralities of circuit passageways and located adjacent to a top metal layer of the m metal layers, said upper metal layer being connected to ~~fewer~~ a predetermined number of top metal layer circuit passageways, the predetermined number of top metal layer circuit passageways being less than all of a plurality of top metal layer circuit passageways of the pluralities of circuit passageways; passageways located through the top metal layer of the m metal layers; and

~~testing said circuit element to identify a desired modification; and~~

modifying said circuit element by connecting said upper metal layer to ~~one of said pluralities of~~ a different set of the plurality of top metal layer circuit

25 passageways located in the top metal layer of the m metal layers, the different set of top metal layer circuit passageways being less than all of the plurality of top metal layer circuit passageways of the pluralities of circuit passageways located through the top metal layer of the m metal layers.

8. (Previously Presented) The IC layout design method of claim 7, wherein at least one of said pluralities of circuit passageways connects through two metal layers.

9. (Previously Presented) The IC layout design method of claim 7, wherein at least one of said pluralities of circuit passageways connects through three metal layers.

10. (Previously Presented) The IC layout design method of claim 7, wherein said standard cell is connected to an intellectual property element.

11. (Previously Presented) The IC layout design method of claim 7, wherein said standard cell is connected to an intellectual property element library.

12. (Previously Presented) The IC layout design method of claim 7, further comprising reserving said upper metal layer exclusively for modification during a subsequent reworking of said circuit element.